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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/830,120	04/23/2004	Jung-hyun Lee	249/456	9015

27849 7590 07/12/2007

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EXAMINER	
STARK, JARRETT J	
ART UNIT	**PAPER NUMBER**
2823	

MAIL DATE	DELIVERY MODE
07/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/830,120	LEE ET AL.	
	Examiner	Art Unit	
	Jarrett J. Stark	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *12-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

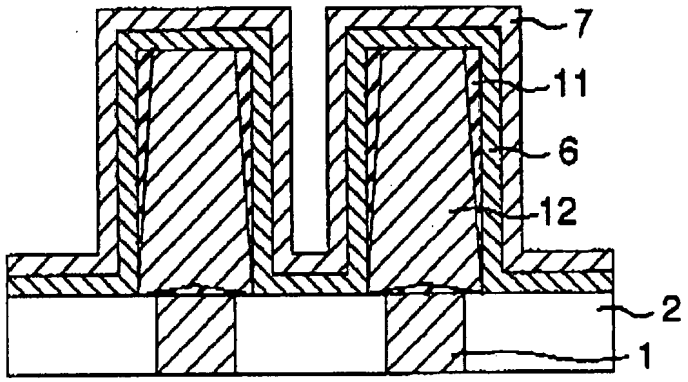
Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 5-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsui et al. (US 6,521,494).

FIG.9d



Regarding claim 1, Matsui et al. discloses a stack-type capacitor comprising:

a lower electrode (Matsui et al, Fig. 9d);

a dielectric layer formed on the lower electrode (Matsui et al, Fig. 9d);

and an upper electrode formed on the dielectric layer (Matsui et al, Fig. 9d);

wherein the lower electrode includes:

a first metal layer having a cylindrical shape and defining a cylindrical space (Matsui et al, Fig. 9d); and

a second metal layer completely filling the cylindrical space defined by the first metal layer (Matsui et al, Fig. 9d).

Regarding claim 5, Matsui et al. discloses a semiconductor memory device including a stack-type capacitor, the device comprising a transistor and a capacitor, wherein the capacitor includes: (Matsui et al, Abstract)

a lower electrode (Matsui et al, Fig. 9d);

a dielectric layer formed on the lower electrode (Matsui et al, Fig. 9d);

and an upper electrode formed on the dielectric layer (Matsui et al, Fig. 9d);

wherein the lower electrode includes:

a first metal layer having a cylindrical shape and defining a cylindrical space (Matsui et al, Fig. 9d);

a second metal layer completely filling the cylindrical space defined by the first metal layer (Matsui et al, Fig. 9d);

Regarding claim 6, Aoki et al. discloses the device as claimed in claim 5, wherein the transistor is electrically connected to the capacitor by a conductive plug (Matsui et al, Fig. 15).

Regarding claims 7 & 8, Aoki et al. discloses the device as claimed in claim 6, wherein a diffusion barrier layer is formed between the lower electrode and the conductive plug (Matsui et al, Col. 1, lines 46-63);

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-4 and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsui et al. (US 6,521,494). in view of Kim et al. (US 2001/00544730).

Regarding claims 2 & 9, Matsui discloses the capacitor as claimed in claim 1 & 5, wherein the first metal layer is a ruthenium layer and however does not disclose that the second metal layer is a nitride and aluminum layer.

Kim discloses wherein the metal layers of the capacitor can be formed from Ru and TaAlN (Kim, paragraph [0013]).

The two references are analogous art because they are from the same field of endeavor of forming a cylindrical stack type capacitor.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use TaAlN to form the metal layers of the stack capacitor, since it has been held to be within the general skill of a worker in the art to select a known material on the base of its suitability, for its intended use involves only ordinary skill in the art. *In re Leshin*, 125 USPQ 416.

Therefore, it would have been obvious to combine Kim with Matsui to obtain the invention as specified.

lower electrode in a capacitor according to the embodiment of the present invention is formed of a refractory metal such as Ti, Ta and W or a refractory metal compound such as TiN, TiSiN, TiAlN, TaN, TaSiN, TaAlN and WN. In particular, when the lower electrode 10 has a three-dimensional structure such as a cylindrical shape, a refractory metal or refractory metal compound deposited by CVD or ALD providing good step coverage is preferable. (Kim, paragraph [0031])

Regarding claim 3 & 10, Matsui in view of Kim disclose the capacitor as claimed in claim 2 & 9, wherein the nitride and aluminum layer is a titanium aluminum nitride layer or a tantalum aluminum nitride layer. (Kim, paragraph [0031])

Regarding claim 4 & 11, Matsui in view of Kim disclose the capacitor as claimed in claim 2 & 9, wherein the upper electrode is a ruthenium layer. (Matsui, Fig. 9d and Kim, paragraph [0013])

Claims 1 and 5-8 are also rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al. (US 2002/0072191).

Regarding claim 1, Aoki et al. discloses a stack-type capacitor comprising:

a lower electrode; (Aoki et al, Fig. 2 layers 5&6)

a dielectric layer formed on the lower electrode; (Aoki et al, Fig. 2 ref # 7)

and an upper electrode formed on the dielectric layer, (Aoki et al, Fig. 3 ref # 8)

wherein the lower electrode includes:

a first metal layer having a cylindrical shape and defining a cylindrical space; and (Aoki et al, Fig. 2 ref # 6)

a second metal layer completely filling the cylindrical space defined by the first metal layer (Aoki et al, Fig. 3 layer 6 completely fills in the top surface of metal layer 5))

Fig. 2

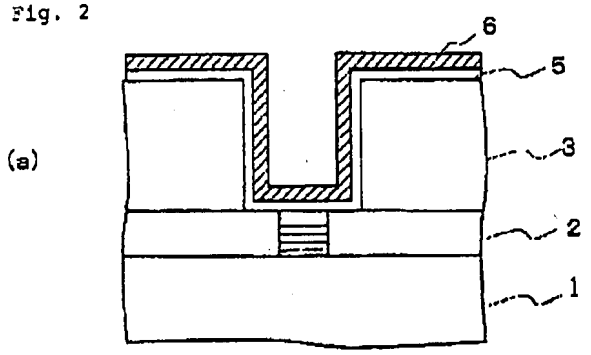
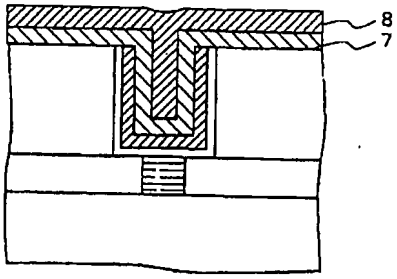


Fig. 3



The shape of a capacitor's electrodes is merely a matter of design choice. The capacitance of a capacitor is proportional to the surface area of the conducting plate and inversely proportional to the distance between the plates. It is also proportional to the permittivity of the dielectric substance that separates the plates. The capacitance of a capacitor is given by:

$$C \approx \frac{\varepsilon A}{d}; A \gg d^2$$

where ε is the permittivity of the dielectric, *A* is the area of the plates and *d* is the spacing between them. Thus, the area A and the spacing d are merely optimized for the desired size and shape inorder to meet specivic design specifications.

"When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill in the art has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense." KSR Int'l Co v. Teleflex Inc.

Regarding claim 5, Aoki et al. discloses a semiconductor memory device including a stack-type capacitor, the device comprising a transistor and a capacitor, wherein the capacitor includes: (Aoki et al, paragraph [0032])

a lower electrode; (Aoki et al, Fig. 2 ref #'s 5&6)

a dielectric layer formed on the lower electrode; (Aoki et al, Fig. 2 ref # 7)

and an upper electrode formed on the dielectric layer, (Aoki et al, Fig. 3 ref # 8)

wherein the lower electrode includes:

a first metal layer having a cylindrical shape and defining a cylindrical space; and (Aoki et al, Fig. 2 ref # 6)

a second metal layer completely filling the cylindrical space defined by the first metal layer (Aoki et al, Fig. 3 ref # 8)

Regarding claim 6, Aoki et al. discloses the device as claimed in claim 5, wherein the transistor is electrically connected to the capacitor by a conductive plug. (Aoki et al, paragraph [0032])

Regarding claims 7 & 8, Aoki et al. discloses the device as claimed in claim 6, wherein a diffusion barrier layer is formed between the lower electrode and the conductive plug (Aoki et al, paragraph [0032]).

Claims 2-4 and 9-11 are also rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al. (US 2002/0072191) in view of Kim et al. (US 2001/00544730).

Regarding claims 2 & 9, Aoki discloses the capacitor as claimed in claim 1 & 5.

Aoki does not expressly disclose wherein the first metal layer is a ruthenium layer and the second metal layer is a nitride and aluminum layer.

Kim discloses wherein the metal layers of the capacitor can be formed from Ru and TaAlN (Kim, paragraph [0013]).

The two references are analogous art because they are from the same field of endeavor of forming a cylindrical stack type capacitor.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use TaAlN to form the metal layers of the stack capacitor, since it has been held to be within the general skill of a worker in the

art to select a known material on the base of its suitability, for its intended use involves only ordinary skill in the art. *In re Leshin*, 125 USPQ 416.

Therefore, it would have been obvious to combine Kim with Aoki to obtain the invention as specified.

> lower electrode in a capacitor according to the embodiment of the present invention is formed of a refractory metal such as Ti, Ta and W or a refractory metal compound such as TiN, TiSiN, TiAlN, TaN, TaSiN, TaAlN and WN. In particular, when the lower electrode 10 has a three-dimensional structure such as a cylindrical shape, a refractory metal or refractory metal compound deposited by CVD or ALD providing good step coverage is preferable. (Kim, paragraph [0031])

Regarding claim 3 & 10, Aoki in view of Kim disclose the capacitor as claimed in claim 2 & 9, wherein the nitride and aluminum layer is a titanium aluminum nitride layer or a tantalum aluminum nitride layer. (Kim, paragraph [0031])

Regarding claim 4 & 11, Aoki in view of Kim disclose the capacitor as claimed in claim 2 & 9, wherein the upper electrode is a ruthenium layer. (Kim, paragraph [0013])

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jarrett J. Stark whose telephone number is (571) 272-6005. The examiner can normally be reached on Monday - Thursday 7:00AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jarrett J Stark
Examiner
Art Unit 2823

JJS
June 20, 2007

MICHELLE ESTRADA
PRIMARY EXAMINER